CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A magnetic memory element comprising:

a pinned ferromagnetic layer;

an antiferromagnetic layer for pinning the pinned ferromagnetic layer;

a free ferromagnetic layer;

a barrier layer separating the pinned and the free layers; and

an offset ferromagnetic layer on a side of the antiferromagnetic layer opposite the pinned ferromagnetic layer, the offset ferromagnetic layer reducing demagnetization coupling between the free and pinned ferromagnetic layers.

2. A memory element as in claim 1, wherein the pinning layer is made up of one of IrMn and PtMn.

3. A memory element as in claim 1, wherein at least one of the free and pinned layers comprises a layer of at least one of Co-Fe and Ni-Fe.

4. A memory element as in claim 1, further comprising conductive layers in electrical contact with the free layer and the offset layer.

5. A magnetic tunnel junction device having memory elements comprising:

a pinned ferromagnetic layer;

an antiferromagnetic layer for pinning the pinned ferromagnetic layer;

a free ferromagnetic layer;

a tunnel junction barrier layer separating the pinned and the free layers; and

an offset ferromagnetic layer on a side of the antiferromagnetic pinning layer opposite the pinned ferromagnetic layer, the offset ferromagnetic layer reduces demagnetization coupling between the free and pinned ferromagnetic layers.

6. A magnetic tunnel junction device as in claim 5, wherein the pinning layer comprises a layer of at least one of IrMn and PtMn.

7. A magnetic tunnel junction device as in claim 5, wherein at least one of the free and pinned layers comprises a layer of at least Co-Fe and Ni-Fe.

8. A memory element as in claim 5, further comprising conductive layers in electrical contact with the free layer and the offset layer.

9. A magnetic random access memory including an array of memory elements, each memory element comprising:
a pinned ferromagnetic layer;

a free ferromagnetic layer;

a barrier layer separating the pinned and the free layers; and

an offset ferromagnetic layer for deflecting flux coupling between the free and pinned ferromagnetic layers.

10. A magnetic random access memory as in claim 9, wherein the pinning layer in each memory element comprises a layer of at least one of IrMn and PtMn.

11. A magnetic random access memory as in claim 9, wherein at least one of the free and pinned layers comprises a layer of at least of one of Co-Fe and Ni-Fe.

12. A magnetic random access memory as in claim 9, further comprising conductive layers in electrical contact with the free layer and the offset layer.

13. A processor system comprising:

a processor; and

a magnetic random access memory device for exchanging data with the processor, the memory device comprising an array of memory element, each comprising:

a pinned ferromagnetic layer;

an antiferromagnetic layer for pinning the pinned ferromagnetic layer;

a free ferromagnetic layer;

a barrier layer separating the pinned and the free layers; and

an offset ferromagnetic layer on a side of the antiferromagnetic layer opposite the pinned ferromagnetic layer, the offset ferromagnetic layer reducing demagnetization coupling between the free and pinned ferromagnetic layers.

14. A processor system comprising:

a processor; and

a magnetic random access memory device for exchanging data with the processor, the memory device comprising an array of memory element, each comprising:

a barrier layer separating the pinned and the free layers; and

an offset ferromagnetic layer for deflecting flux coupling between the free and pinned ferromagnetic layers

15. A method of forming a magnetic tunnel junction element comprising:

forming a free ferromagnetic layer;

forming a pinned ferromagnetic layer,

forming a tunnel junction barrier layer between the free and pinned layers;

forming another ferromagnetic layer in flux communication with the pinned layer which reduces demagnetization coupling between the pinned ferromagnetic layer and the free ferromagnetic layer.

16. A method as in claim 15, wherein the pinning layer comprises a layer of at least one of IrMn and PtMn.

17. A method as in claim 15, wherein at least one of the free and pinned layers comprises a layer of at least one of Co-Fe and Ni-Fe.

18. A method as in claim 15, further comprising forming conductive layers in electrical contact with the free layer and the offset layer.

19. A method of forming a magnetic memory element comprising:

forming a free ferromagnetic layer;

forming a pinned ferromagnetic layer;

forming a tunnel junction barrier layer between the free and pinned layers;

forming an antiferromagnetic layer for pinning the pinned layer; and

forming another ferromagnetic layer on a side of said antiferromagnetic layer which is opposite a side forming said pinned layer, said another ferromagnetic layer receiving flux coupling between said free and pinned layers.